IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application: **DeWitt, Jr. et al.**	§	Group Art Unit: **2193**
	§	
Serial No.: **10/675,776**	§	Examiner: **Vu, Tuan A.**
	§	
Filed: **September 30, 2003**	§	Confirmation No.: **6262**
	§	
For: **Method and Apparatus for Counting Execution of Specific Instructions and Accesses to Specific Data Locations**	§	Attorney Docket No.: **AUS920030481US1**

35525
PATENT TRADEMARK OFFICE
CUSTOMER NUMBER

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

REASONS IN SUPPORT OF APPLICANTS' PRE-APPEAL BRIEF REQUEST FOR REVIEW

Sir:

This document is submitted in support of the Pre-Appeal Brief Request for Review filed concurrently with a Reinstatement of Appeal in compliance with 37 C.F.R. 41.31 and with the rules set out in the OG of July 12, 2005 for the New Appeal Brief Conference Pilot Program.

No fee or extension of time is believed due for this request. However, if any fee or extension of time for this request is required, Applicants request that this be considered a petition therefor. The Commissioner is hereby authorized to charge any additional fee, which may be required, or credit any refund to IBM Corporation Deposit Account No. 09-0447.

REMARKS

Applicants hereby request a Pre-Appeal Brief Review (hereinafter "Request") of the claims finally rejected in the Final Office Action mailed June 15, 2010. The Request is provided herewith in accordance with the rules set out in the OG dated July 12, 2005.

With regard to the allowed claims, the Examiner states the following:

> Claims 1, 32 stand rejected in the Double patenting Rejection as set forth above; yet contain allowable subject matter in view of the teachings provided via Fig. 31 of the Specifications; but would be allowable if rewritten in a form including or reasonably conveying functionality of all of the constituents (see Note below) of the 'instruction cache unit' described in the pertinent section. The allowable subject matter revolves around the following scenario, pending the inclusion of *range registers, counter increment based on range execution* of Figure 31:
>
> A instruction cache unit (ICU) having a counter therein that is incremented responsive to this ICU receiving of a spare bit and an instruction, the spare bit as an indicator to be determined by the ICU as to whether the instruction to be one to be monitored by a performance monitor unit, wherein upon receiving a signal from the ICU in response to the determination, the performance unit increments a counter implemented inside the ICU in conjunction with sending by the ICU of the instruction to a functional unit.
>
> Note: the constituents of the ICU depicted in **Figure 31,** deemed allowable based on the previously considered Appeal Brief (per 913012009), based on the emphasis expressed therein by the arguments regarding the Inventor's particular way of implementing an "instruction cache unit" being distinguishable over any conventional instruction cache, include (see Specifications):
>
> In this example, program 3100 includes instruction range 3102 and 3104. Each of these ranges has been identified as ones of interest for monitoring. Each of these ranges is set within an instruction unit, such as instruction cache unit 214 in FIG. 2. Each range is used to tell the processor the number of instructions executed in a range, as well as the number of times a range is entered during execution of program 3100.
>
> Instruction cache unit 3106 uses range registers 3108 to define instruction ranges. These registers may be existing registers or instruction cache unit 3106 may be modified to include registers to define instruction ranges. These ranges may be based on addresses of instructions. Additionally, range registers 3108 may be updated by various debugger programs and performance tools.
>
> If an instruction is executed in a range, such as instruction range 3102 or instruction range 3104, a counter is incremented in instruction cache unit 3106.

Final Office Action dated June 15, 2010, pages 5-6.

Applicants have submitted terminal disclaimers, thus overcoming the Examiner's Double Patenting Rejection. However, the Applicants respectfully submit that the Examiner's requirement that the Applicants rewrite the claims is improper. The Examiner has not cited any Rule, Law or Prior Art that would necessitate amendments to the claims. Instead, the Examiner's attempt to require additional limitations amounts to an improper limitation on the scope of the claims.

Because the Examiner has not cited any Rule, Law or Prior Art that would necessitate amendments to the claims, the Examiner's requirement that the Applicants rewrite the claims is improper and should be withdrawn.

The Pre-Appeal Brief Conference Panel is invited to call the undersigned at the below-listed telephone number if, in the opinion of the Panel, such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: September 15, 2010

Respectfully submitted,

/Brandon G. Williams/

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